

Uva Wellassa University of Sri Lanka
Faculty of Science and Technology
Department of Computer Science and Technology
100 Level 2nd Semester Examination – Jan. / Feb. 2016
CST 131-2 Microcomputer Architecture and Logic Design



Instructions to candidates:

Duration: Two (02) hours

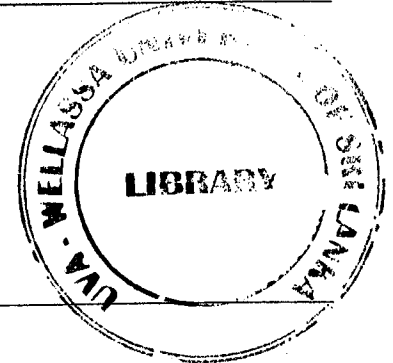
Number of questions: Four (04)

Answer all questions

Mark allocation: 100

Calculators are **allowed**.

This paper consist of two (02) parts: Part – A and Part – B.



Part – A

1.
 - a.
 - i. Express the binary number 10110.01 in decimal. (3 mark)
 - ii. Convert $(18.625)_{10}$ to binary. (5 mark)
 - b.
 - i. Given the two binary numbers $X = 11101_2$ and $Y = 01011_2$, perform the subtraction of $X - Y$ using **2's complement**. (5 mark)
 - ii. **(r-1)'s complement** of any number system is given by the a general formula $\{(r^n)_{10} - 1\} - N$
where, r = Radix or base of the number system,
 n = Number of digits
 N = Number.
Find **10's complement** of decimal number 456 using the general formula.
(Hint: In order to find 10's complement of 456, you are required to find 9's complement of it). (5 mark)
 - c. Express the **BCD (Binary Coded Decimal)** code for the hexadecimal number $(9F)_{16}$. (5 mark)
 - d. What is the **Gray Code** for seven (7)? (2 mark)
2.
 - a. State the **DeMorgan's theorem** for Boolean expressions. (2 mark)
 - b. Simplify the following Boolean expressions to a minimum number of literals. Clearly state the intermediate steps and the rules used.
 - i. $AB + A(B + C) + B(B + C)$
 - ii. $A + AB + \overline{A}BC$
 - iii. $A + (A + \overline{C})(A + B)$(9 mark)
 - c. Simplify the following Boolean expressions, using **Karnaugh maps**.
 - i. $\overline{A}\overline{B} + AB$

- ii. $\overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$ (10 mark)
- d. Construct a Boolean expression that simulates the functionality of **XOR addition**. The expression must be comprised of only basic operations such as AND, NOT and OR. (4 mark)
- 3.
- a. A machine has 4 fail-safe sensors. The machine should keep running unless any of the following conditions arise:
- If sensor 1 is activated.
 - If sensor 2 and sensor 4 are activated together.
 - If sensor 3 and sensor 4 are activated together.
- i. Derive the truth table for this scenario. (4 mark)
- ii. Simplify the boolean expression for the output using Karnaugh maps. (6 mark)
- ii. Construct a logic gate network to satisfy requirements with basic logic gates. (4 mark)
- iii. Re-design the developed logic gate network with **NAND** gates only. (4 mark)
- b.
- i. Distinguish **combinational** and **sequential** logic circuits. (2 mark)
- ii. What are the **two (02)** major types of sequential circuits? (2 mark)
- c. List any **three (03)** applications of JK flip-flops. (3 mark)
- 4.
- a.
- i. What is meant by a ripple counter? (2 mark)
- ii. Implement a **three (3) bit** asynchronous ripple counter using **J-K flip-flops**. (4 mark)
- iii. Discuss the necessity of **synchronous counters** in the context of **cumulative delay**. (3 mark)
- b. Explain how a **BCD** or **decade counter** can be constructed from a **4 bit ripple counter**. (4 mark)
- c.
- i. Why we need **full-adder** while the **half-adder** is capable of performing bit wise addition? (2 mark)
- ii. Construct a full-adder using **two (02) half adder** units. (4 mark)
- iii. Explain how a **4 bit full-adder** can be converted in to a **subtractor**. (4 mark)
- d. Differentiate **Multiplexers** against **Demultiplexers**. (2 mark)